Chapter 6: Field-Effect Transistors (FETs)

The Field-Effect Transistor

The **field-effect transistor (FET)** is a semiconductor device, which depends for its operation on the control of current by an electric field. Today FETs are the most widely used components in integrated circuits. There are two of field effect transistors:

1. **JFET** (Junction Field-Effect Transistor).
2. **MOSFET** (Metal Oxide Semiconductor Field Effect Transistor).

The FET has several advantages over conventional transistor.

1. In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor. In FET the operation depends upon the flow of majority carriers only. It is called **unipolar device**.
2. The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hence the high input impedance of the order of M ohm.
3. It is less noisy than a bipolar transistor.
4. It exhibits no offset voltage at zero drain current.
5. It has thermal stability.
6. It is relatively immune to radiation.

The main disadvantage is its relatively small gain bandwidth product in comparison with conventional transistor.

Junction Field-Effect Transistor

The JFET is a type of FET that operates with a reverse-biased pn junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, n channel or p channel.

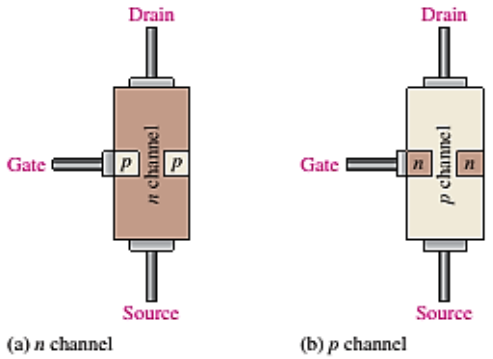


Figure 1: A representation of the basic structure of the two types of JFET.

Figure 1(a) shows the basic structure of an n-channel JFET. Wire leads are connected to each end of the n-channel; the **drain** is at the upper end (analogous to the collector of

a BJT), and the **source** is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the **gate** (analogous to the base of a BJT) lead. For simplicity, the gate lead is shown connected to only one of the p regions.

Operation of JFET

To illustrate the operation of a JFET, Figure 2 shows dc bias voltages applied to an n-channel device, when the drain is positive with respect to the source and there is no gate-source voltage, there is current in the channel. When a negative gate voltage is applied to the FET, the electric field causes the channel to narrow, which in turn causes current to decrease.

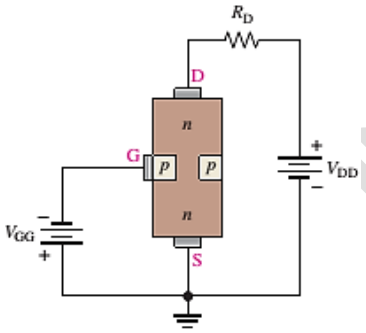


Figure 2: A biased n-channel JFET.

The symbol for an n-channel JFET is shown, along with the proper polarities of the applied dc voltages. For an n-channel device, the gate is always operated with a negative (or zero) voltage with respect to the source.

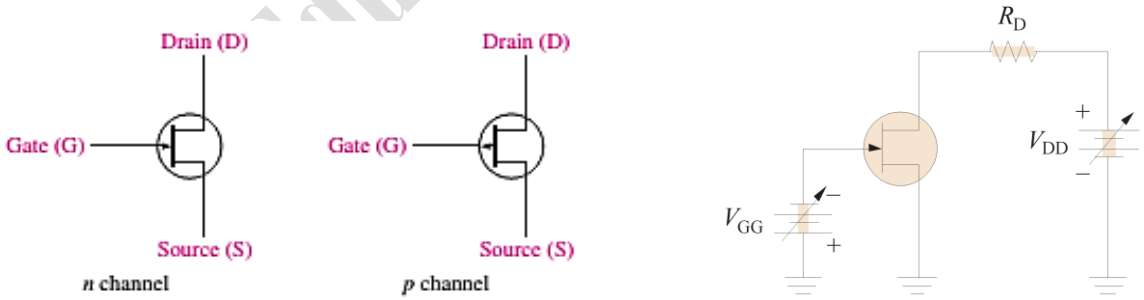


Figure 3: JFET schematic symbols.

JFET characteristics and parameters

There are three regions in the characteristic curve for a JFET as illustrated for the case when V_{GS}=0V. Between A and B is the **Ohmic region**, where current and voltage are related by Ohm's law. From B to C is the **active** (constant-current) **region** where current is essentially independent of V_{DS}. Beyond C is the **breakdown region**. Operation here can damage the FET.

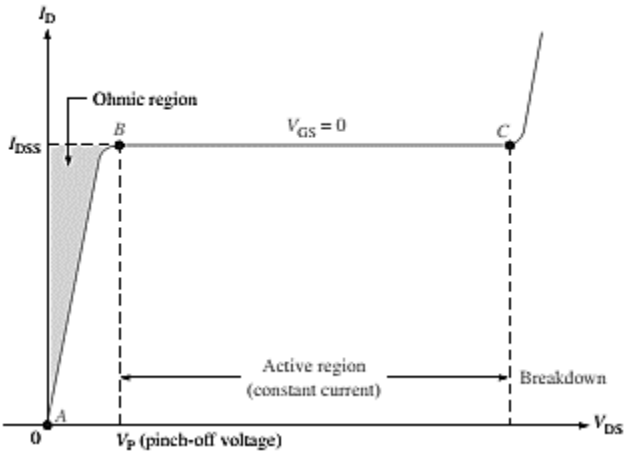


Figure 4: The drain characteristic curve of a JFET for V_{GS}=0.

When V_{GS} is set to different values, the relationship between V_{DS} and I_D develops a family of characteristic curves for the device. An n-channel characteristic is illustrated Figure 5. Notice that V_p is positive and has the same magnitude as $V_{GS(off)}$.

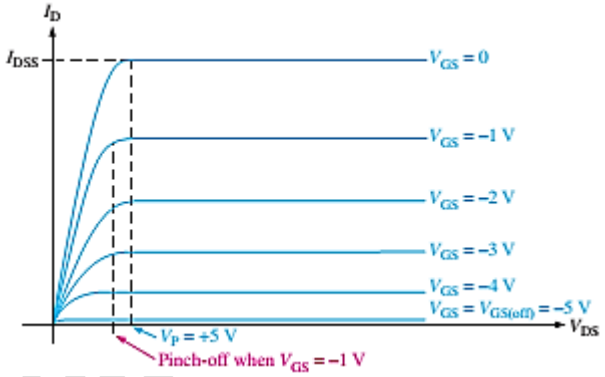


Figure 5: Family of drain characteristic curves.

JFET Universal Transfer Characteristic

A plot of V_{GS} to I_D is called the transfer or transconductance curve. The transfer curve is a is a plot of the output current (I_D) to the input voltage (V_{GS}).

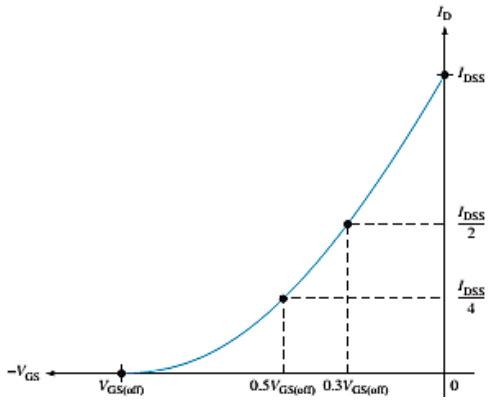


Figure 6: JFET universal transfer characteristic curve (n-channel).

The transfer curve is based on the equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

By substitution, you can find other points on the curve for plotting the universal curve.

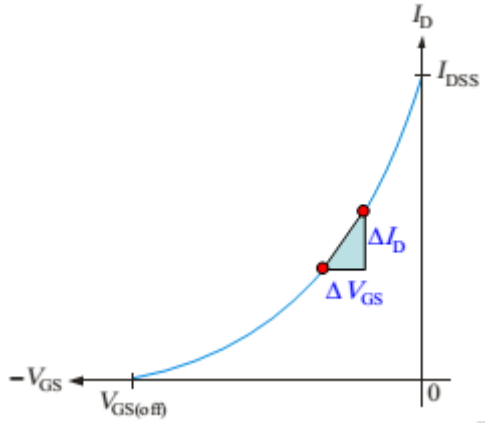


Figure 7: g_m varies depending on the bias point (V_{GS}).

The transconductance (transfer conductance), g_m, is the ratio of a change in output current (ΔI_D) to a change in the input voltage (ΔV_{GS}). This definition is

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The following approximate formula is useful for calculating g_m if you know g_{m0}.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

The value of g_{m0} can be found from

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

Because the slope changes at every point along the curve, the transconductance is not constant, but depends on where it is measured.

The input resistance of a JFET is given by:

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

where I_{GSS} is the current into the reverse biased gate. JFETs have very high input resistance, but it drops when the temperature increases.

Example: A certain JFET has an I_{GSS} of -2nA for V_{GS}=-20V. Determine the input resistance.

Solution: $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{20V}{2nA} = 10G\Omega$

JFET Biasing

Just as with the BJT, the purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point. Three types of bias are self-bias, voltage-divider bias, and current-source bias.

Self-bias

Self-bias is simple and effective, so it is the most common biasing method for JFETs. The JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for a p-channel JFET. This can be achieved using the self-bias arrangements shown in Figure 8. The gate resistor (R_G) does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0V. R_G is necessary only to force the gate to be at 0V and to isolate an ac signal from ground in amplifier applications.

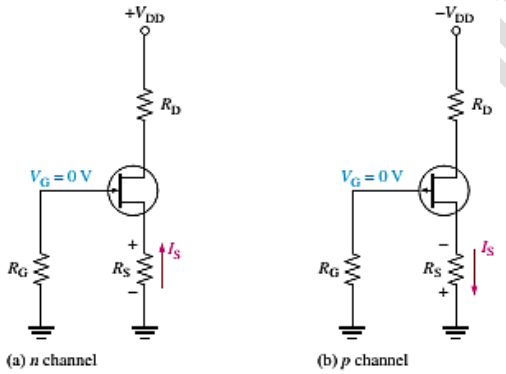


Figure 8: Self-biased JFETs (I_S= I_D in all FETs).

For the n-channel JFET in Figure 8(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since I_S=I_D and V_G=0, then V_S=$I_D R_S$. The gate-to-source voltage is

$$V_{GS}=V_G-V_S = 0 - I_D R_S = - I_D R_S$$

Thus, $$V_{GS} = -I_D R_S$$

For the p-channel JFET shown in Figure 8(b), the current through R_S produces a negative voltage at the source, making the gate positive with respect to the source. Therefore, since I_S =I_D,

$$V_{GS} = +I_D R_S$$

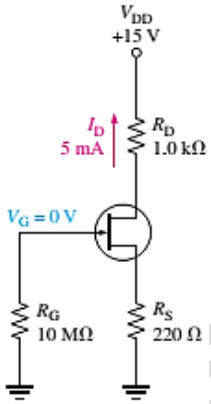
Keep in mind that analysis of the p-channel JFET is the same except for opposite-polarity voltages. The drain voltage with respect to ground is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

Since V_S=$I_D R_S$, the drain-to-source voltage is

$$V_{DS} =V_D-V_S =V_{DD} - I_D(R_D+R_S)$$

Example: For the JFET in the following Figure, the drain current (I_D) is approximately 5 mA. Determine V_{DS} and V_{GS}.



Solution: $V_S=I_DR_S= (5mA)(220Ω)=1.1V$

$V_D = V_{DD}-I_DR_D=15V-(5mA)(1.0kΩ)$

$=15V - 5V=10V$

Therefore, $V_{DS}= V_D - V_S = 10\ V - 1.1\ V =$ **8.9 V**

Since $V_G=0$ V,

$V_{GS} = V_G - V_S = 0\ V - 1.1\ V =$ **-1.1 V**

Voltage-Divider Bias

Voltage-divider biasing is a combination of a voltage-divider and a source resistor to keep the source more positive than the gate. V_G is set by the voltage-divider and is independent of V_S. V_S must be larger than V_G in order to maintain the gate at a negative voltage with respect to the source. Voltage-divider bias helps stabilize the bias for variations between transistors.

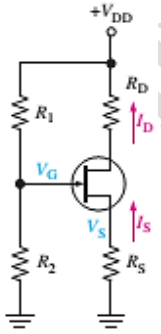


Figure 9: An n-channel JFET with voltage-divider bias ($I_S=I_D$).

Current-Source Bias

An even more stable form of bias is current-source bias. The current-source can be either a BJT or another FET. With current-source biasing, the drain current is essentially independent of V_{GS}.

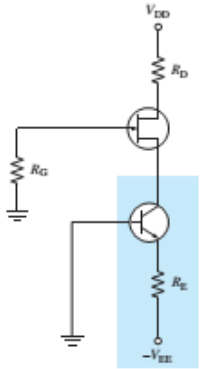


Figure 10: Current-source bias.

In this circuit, Q_2 serves as a current source for Q_1. An advantage to this particular circuit is that the output can be adjusted (using R_{S2}) for 0 V DC.

Example: A current-source bias circuit has the following values: V_{DD}= 9V, V_{EE}=-6V, and R_G=10MΩ. To produce a 10 mA drain current and a 5V drain voltage, determine the values of R_E and R_D.

Solution:

$$R_E = \frac{V_{EE}}{I_D} = \frac{6V}{10mA} = 600\Omega$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{9V - 5V}{10mA} = 400\Omega$$

JFET Ohmic Region

As described before, the ohmic region is between the origin and the active region. A JFET operated in this region can act as a variable resistor. Data from an actual FET is shown. The slopes (which represent conductance) of successive V_{GS} lines are different in the ohmic region. JFETs are often biased in the ohmic region for use as a voltage controlled variable resistor. The control voltage is V_{GS}, and it determines the resistance by varying the Q-point.

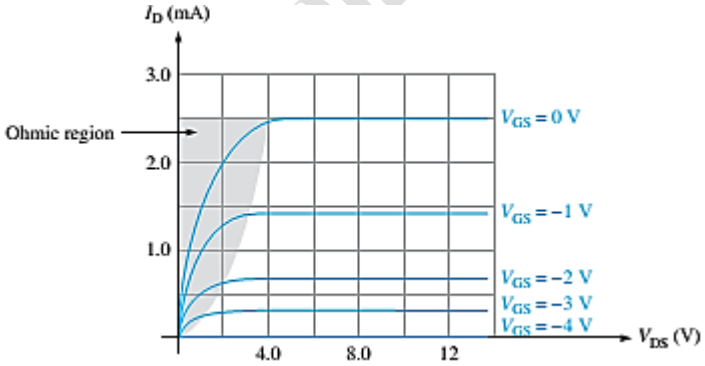


Figure 11: The ohmic region is the shaded area.